FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.: FIS920000227US2	Divisional Application of U.S. Serial No.: 09/885,790
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT: Divakaruni et al.	
(Use several sheets if necessary) (37 CFR 1.98(b))	FILING DATE:	PRIOR ART GROUP: 1765

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
PC	AA	5,895,253	04/20/1999	Akram			
PC	AB	5,998,251	12/07/1999	Wu et al.			
PC	AC	6,030,867	02/29/2000	Chien et al.			
PC	AD	6,265,302	07/24/2001	Lim et al.			
PC	AE	6,344,383	02/05/2002	Berry et al.			
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUB-CLASS	TRANSLATION YES	TRANSLATION NO
	AL							
	AM							
	AN							
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

PC	AQ	"A Novel Trench DRAM Cell with a VERtIcal Access Transistor and BuriEd STrap (VERI BEST) for 4Gb/16Gb", U. Gruening et al., IEDM 99-25, 1999.
PC	AR	"Extending Trench DRAM Technology to 0.15μm Groundrule and Beyond", T. Rupp et al., IEDM 99-33, 1999.
PC	AS	"A 0.135 μm^2 $6F^2$ Trench-Sidewall Vertical Device Cell for 4Gb/16Gb DRAM", C. J. Radens et al., 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 80-81, IEEE, 2000.

EXAMINER	DATE CONSIDERED
[signature]	08/02/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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